CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

AMENDMENTS TO THE CLAIMS

1. (currently amended) A method for testing a fixed logic device formed within a gasket, comprising:

receiving an FPGA scan chain and configuring an FPGA fabric portion for a specified test;

producing a first test signal and a second test signal in the FPGA fabric portion ~~to the fixed logic device~~;

providing the first test signal as input to an isolation circuit element;

providing the second test signal to a programmable interconnect resource;

selecting for input to the fixed logic device between the first signal and the second signal in response to a test mode configured in the FPGA fabric portion;

receiving an output test signal from the fixed logic device;

applying a signature function to the received output test signal;

repeating the producing, receiving and applying steps for a specified number of times; and

determining if a value of the signature function corresponds to an expected value.

2. (original) The method of claim 1 further comprising the step of isolating the fixed logic device that is to be tested.

3. (canceled)

4. (original) The method of claim 1 further comprising the step of receiving an output test signal from the fixed logic device by way of an isolation circuit element.

5. (original) The method of claim 1 wherein the determining step is performed by logic within an FPGA fabric portion.

6. (original) The method of claim 1 wherein the determining step is performed by an external tester.

7. (original) The method of claim 1 wherein the determining step includes the step of comparing the signature to an expected value.

8. (currently amended) An FPGA, comprising:

an FPGA fabric portion;

a Gasket formed at least partially within the FPGA fabric portion, the Gasket forming interfacing logic between an embedded core device and the fabric portion; and

isolation circuitry formed within the Gasket, the isolation circuitry being serially coupled to receive test signals from the FPGA fabric portion, isolate the embedded core device from the Gasket during testing of the embedded core device, and isolate the Gasket from the embedded core device during testing of the Gasket.

9. (currently amended) The FPGA of claim 8 wherein the isolation circuitry includes a multiplexer array, which multiplexer array facilitates sending test signals directly to the embedded core device ~~a device under test~~.

10. (currently amended) The FPGA of claim 8 wherein the isolation circuitry includes a multiplexer array, which multiplexer array facilitates sending test signal outputs directly from the embedded core device ~~a device under test~~ to the FPGA fabric.

11. (currently amended) An FPGA, comprising:

an FPGA fabric portion;

a Gasket formed at least partially within the FPGA fabric portion, the Gasket forming interfacing logic between an embedded core device and the fabric portion;

a first ~~at least one~~ multiplexer coupled to receive a first test signal from the FPGA fabric portion by way of a communication path formed within the Gasket portion, wherein the communication path is accessible while the FPGA is configured for testing at least a portion of the Gasket; and

a fixed logic device formed within the Gasket, the fixed logic device being coupled receive a second test signal from the FPGA fabric portion and provide the second test signal to ~~between~~ the first multiplexer ~~and the FPGA fabric portion~~, wherein the first multiplexer selects between the first test signal received from the FPGA fabric portion and the second test signal for input to the embedded core device in response to a test mode configuration of the FPGA fabric portion.

12 – 14. (canceled)

15. (currently amended) The FPGA of claim 11, further comprising a second ~~wherein the~~ multiplexer ~~is~~ coupled to receive an output~~s~~ signal from an embedded core device and a third test signal from the FPGA fabric portion, and to ~~produce~~ select between the third test signal and the output signal from the embedded core device for input ~~received outputs~~ to the fixed logic device in response to ~~whenever~~ a test mode configuration of the FPGA fabric portion ~~is not configured to test at least a portion of the Gasket~~.

16 – 18. (canceled)

19. (original) An FPGA, comprising:

ID circuitry for delivering a device ID to an embedded device;

input circuitry for receiving test signals from test circuitry; and

multiplexer circuitry coupled to receive input test signals and control signals from the input circuitry and ID information from the ID circuitry, and to produce selected input signals to the embedded device.

20. (original) The FPGA of claim 19 further comprising test circuitry coupled to the input circuitry to produce test and control signals thereto.

21. (original) The FPGA of claim 19 being configurable to connect the input circuitry to pins that may be connected to external test equipment, which external test equipment is for producing test signals that are received by the multiplexer circuitry and conducted to the inputs of the embedded device.

22. (currently amended) An FPGA configured in a test mode of operation, comprising:

an FPGA fabric portion;

a Gasket formed at least partially within the FPGA fabric portion, the Gasket forming interfacing logic between an embedded core device and a subset of the FPGA fabric portion;

a first multiplexer coupled to receive a first test signal from the FPGA fabric portion by way of a communication path formed within the Gasket portion, wherein the communication path is accessible while the FPGA is configured for testing at least a portion of the Gasket;

a fixed logic device formed within the Gasket, the fixed logic device being coupled to receive a second test signal from the FPGA fabric portion and provide the second test signal to the first multiplexer, wherein the first multiplexer selects between the first test signal received from the FPGA fabric portion and the second test signal for input to the embedded core device in response to a test mode configuration of the FPGA fabric portion;

first logic circuitry forming a plurality of latches for receiving an FPGA scan chain containing test vectors;

second logic circuitry forming a test output signature generator;

third logic circuitry configured for performing a specified test; and

fourth logic circuitry for determining whether the FPGA passed or failed a test.

23. (currently amended) The FPGA of claim 22 wherein each of the first, second and third logic circuitry are formed to communication with the ~~a~~ fixed logic device ~~within an FPGA Gasket~~.

24. (canceled)

25. (currently amended) The FPGA of claim 23 wherein the fixed logic device is an embedded core processor ~~that is embedded within the Gasket~~.

26 – 31. (canceled)

32. (currently amended) A programmable logic device (PLD), comprising:
an integrated circuit, including,

a configuration memory arranged for storage of bit values that program functions of programmable logic resources and programmable interconnect resources of the PLD;

a plurality of programmable logic resources coupled to the configuration memory;

a plurality of programmable interconnect resources coupled to the configuration memory and to the programmable logic resources;

a fixed logic circuit; and

an interface circuit including,

a plurality of programmable switches coupled to the subset of the programmable interconnect resources;

a fixed interface circuit coupled to the plurality of switches; and

a selector circuit arrangement coupled to the fixed interface circuit, to the fixed logic circuit, and to the interconnect resources, the selector circuit arrangement adapted to, for input to each of a plurality of input pins of the fixed logic circuit, select between a signal from the fixed interface and ~~a~~ an signal from the interconnect resources.

33. (previously presented) The PLD of claim 32, wherein the selector circuit is further adapted to, for input to each of a plurality of input ports of the fixed interface circuit, select between a signal from an output port of the fixed logic circuit and a signal received from the interconnect resources.

34. (previously presented) The PLD of claim 33, wherein:

the integrated circuit further includes a non-volatile memory adapted for storage of a device identifier; and

the interface circuit further includes an ID selector circuit arrangement coupled to the fixed logic circuit, to the interconnect resources, and to the non-volatile memory, the ID selector circuit arrangement adapted to, for input to each of at least two input ports of the fixed logic circuit, select between a signal received from the interconnect resources and a signal received from the non-volatile memory.

35. (previously presented) The PLD of claim 33, wherein the fixed logic core is a microprocessor.